What is claimed is:

1. A voltage detection circuit comprising a first MOS transistor whose gate and drain are connected with a first node, a second MOS transistor whose gate and drain are connected with the first node and a third node, respectively, a first resistive element which is connected between the first node and a second node, a second resistive element which is connected between the second node and a ground voltage terminal, a first NOT circuit whose input terminal is connected with the second node, whose output terminal is a fourth node, and which is connected between the third node and the ground voltage terminal, and a second NOT circuit whose input terminal is connected with the fourth node and whose output terminal is a fifth node.

2. A voltage detection circuit comprising a first MOS transistor whose gate and drain are connected with a first node, a second MOS transistor whose gate and drain are connected with the first node and a third node, respectively, a first resistive element which is connected between the first node and a second node, a second resistive element which is connected between the second node and a ground voltage terminal, a first NOT circuit whose input terminal is connected with the second node and whose output terminal is a fourth node, a second NOT circuit whose input terminal is connected with the fourth node, whose output terminal is

a fifth node, and which is connected between a third node and the ground voltage terminal, and a third MOS transistor whose gate is connected with the fifth node and which is connected between either the ground voltage terminal or the power-supply voltage terminal and the fourth node.

3. The voltage detection circuit of claim 2, wherein the first, second, and third MOS transistors are P-channel type MOS transistors, and the source of the third MOS transistor is connected with a power-supply voltage terminal.

4. A voltage detection circuit comprising a first voltage detection circuit which detects a first voltage and outputs a first signal and a second voltage detection circuit which detects a second voltage lower than the first voltage and outputs a second signal, wherein the first voltage detection circuit comprises a first P-channel type MOS transistor whose gate and drain are connected with a first node, a second P-channel type MOS transistor whose gate and drain are connected with the first node and a third node, respectively, a first resistive element which is connected between the first node and a second node, a second resistive element which is connected between the second node and a ground voltage, a NOT circuit whose input terminal is the second node, whose output terminal is a fourth node, and which is connected between the third node and the ground

voltage terminal, and a third MOS transistor which is connected between either the ground voltage terminal or a power-supply voltage terminal and the fourth node and whose gate is applied with the second signal of the second voltage detection circuit.

5. The voltage detection circuit of claim 4 characterized in that the second signal which is outputted from the second voltage detection circuit is outputted only when the power supply is turned on.

6. The voltage detection circuit of claim 4, wherein the second signal which is outputted from the second voltage detection circuit is outputted for a certain time period after the power supply is turned on.

7. A voltage detection circuit characterized by comprising a first P-channel type MOS transistor whose gate and drain are connected with a first node, a second P-channel type MOS transistor whose gate and drain are connected with the first node and a third node, respectively, a first resistive element which is connected between the first node and a second node, a second resistive element which is connected between the second node and a ground voltage terminal, an N-channel type MOS transistor whose gate is connected with the second node, and a first NOT circuit whose input is the third node and whose output is a fourth node.

8. The voltage detection circuit of claim 7

characterized in that the first resistive element is an N-channel type MOS transistor.

9. A power-on/off reset circuit characterized by comprising a first voltage detection circuit which detects a first voltage and outputs a first signal, and preventing a new operational sequence and continuing an on-going sequence when a power-supply voltage is equal to or lower than the first voltage.

10. A semiconductor device comprising a first circuit which executes a series of operational sequences in accordance with a starting signal, and a power-on/off reset circuit including a first voltage detection circuit which detects a first voltage and outputs a first signal, and preventing a new operational sequence from starting in the first circuit when a power-supply voltage is equal to or lower than the first voltage.

11. A semiconductor device comprising a first circuit which executes a series of operational sequences in accordance with a starting signal, and a power-on/off reset circuit including a first voltage detection circuit which detects a first voltage and outputs a first signal, and preventing the first circuit from being suspended until the series of operational sequences which are already being executed are completed when a power-supply voltage is equal to or lower than the first voltage.

12. A power-on/off reset circuit characterized by comprising a first voltage detection circuit which detects a first voltage and outputs a first signal, and a second voltage detection circuit which detects a second voltage lower than the first voltage and outputs a second signal, preventing a new operational sequence when a power-supply voltage is equal to or lower than the first voltage, and immediately suspending an operation when the power-supply voltage is equal to or lower than the second voltage.

13. A power-on/off reset circuit characterized by comprising a first voltage detection circuit which detects a first voltage and outputs a first signal, and a second voltage detection circuit which detects a second voltage lower than the first voltage and outputs a second signal, and a time for a power-supply voltage to drop from the first voltage to the second voltage being longer than a predetermined operational sequence completion time.

14. A voltage detection circuit characterized by comprising a first voltage detection circuit which (a) detects a first voltage and outputs a first signal, (b) outputs the first signal only when the power supply is turned on, and (c) outputs the first signal for a certain time period after the power supply is turned on, a second voltage detection circuit which detects a second voltage and outputs a second signal, a third voltage detection circuit which

detects a third voltage higher than the second voltage, a fourth voltage detection circuit which detects a fourth voltage higher than the third voltage and outputs a fourth signal, a signal selection circuit which selects either the third signal or the fourth signal and outputs a fifth signal, a first control circuit which generates an OR output of the first signal and the second signal, and a second control circuit which generates an OR output of the first signal and the fifth signal.

15. A power-on/off reset circuit characterized by comprising a voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage, and outputs a first signal, the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops, and a new operational sequence being prevented when the power-supply voltage is equal to or lower than a voltage for the first signal to be transmitted.

16. A power-on/off reset circuit characterized by comprising a first voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage, and outputs a first signal, and a second voltage detection circuit which detects a third voltage which is lower than the first voltage and outputs a second signal,

the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops, a new operational sequence being prevented when the power-supply voltage is equal to or lower than a voltage for the first signal to be transmitted, and an operation being immediately suspended when the power-supply voltage is equal to or lower than the third voltage.

17. A power-on/off reset circuit characterized by comprising a first voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage and outputs a first signal, and a second voltage detection circuit which detects a third voltage which is lower than the first voltage and outputs a second signal, the first signal being transmitted at the second voltage when a power-supply voltage rises and transmitted at the first voltage when the power-supply voltage drops, a time for a power-supply voltage to drop from the first voltage to the third voltage being longer than a predetermined operational sequence completion time.

18. A semiconductor device comprising a non-volatile memory and a power-on/off reset circuit including a first voltage detection circuit which detects a first voltage and outputs a first signal, preventing a new operational sequence, and continuing an on-going sequence when a

power-supply voltage is equal to or lower than the first voltage, wherein

the semiconductor device is characterized by not operating the non-volatile memory when the power-supply voltage is equal to or lower than the first voltage.

19. A semiconductor device comprising a non-volatile memory and a power-on/off reset circuit including a first voltage detection circuit which detects a first voltage and outputs a first signal, and a second voltage detection circuit which detects a second voltage which is lower than the first voltage and outputs a second signal, preventing a new operational sequence when a power-supply voltage is equal to or lower than the first voltage, and immediately suspending an operation when the power-supply voltage is equal to or lower than the second voltage, wherein

the semiconductor device is characterized by not operating the non-volatile memory when the power-supply voltage is equal to or lower than the second voltage.

20. A semiconductor device comprising a non-volatile memory and a power-on/off reset circuit including a voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage and outputs a first signal, the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops,

and preventing a new operational sequence when the power-supply voltage is equal to or lower than a voltage for the first signal to be transmitted, wherein

the semiconductor device is characterized by not operating the non-volatile memory when the power-supply voltage is equal to or lower than the first voltage or equal to or lower than the third voltage.

21. A semiconductor device comprising a non-volatile memory and a power-on/off reset circuit characterized by comprising a first voltage detection circuit which detects a first voltage and a second voltage higher than the first voltage and outputs a first signal, and a second voltage detection circuit which detects a third voltage which is lower than the first voltage and outputs a second signal, the first signal being transmitted at the second voltage when a power-supply voltage rises, and transmitted at the first voltage when the power-supply voltage drops, preventing a new operational sequence when a power-supply voltage is equal to or lower than the voltage for the first signal to be transmitted, and immediately suspending an operation when the power-supply voltage is equal to or lower than the third voltage, wherein

the semiconductor device is characterized by not operating the non-volatile memory when the power-supply voltage is equal to or lower than a voltage for the first

signal to be transmitted or equal to or lower than the third voltage.